REMARKS

Claims 1-27 remain in the application. Claims 1, 11, 17 and 25 have been amended.

Claim Rejections under 35 U.S.C. § 102(b)

Claims 1-5, 11, 17-19 and 25-27 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,161,166 to Doing et al. ("Doing").

Embodiments of the present invention pertain to reducing a size of a linear address of an instruction. Using the full linear address to access an array, such as a tag array results in the tag array storing addresses having the same size as the full linear address. By reducing the size of the linear address, the size of the tag array may be reduced as well. In the example of Figure 1, the reduction module 46 receives a full linear address from the processor bus and using bits of the full linear address reduces the size of the full linear address from 32 bits to 23 bits. Once of example of this is through a hashing operation where bits 32a and bits 32b are hashed down to create a lesser number of bits 30. In this example, twenty bits of the full linear address are hashed down to ten bits used in the reduced linear address 28. The independent claims have been amended to specifically recite that bits of the full linear address are used to generate a lesser number of bits.

Such a feature is not shown in Doing. Though Doing describes a 64 bit effective address, Doing does not provide for a reduction in the number of bits in the effective address as recited in the claims. As stated in the Office Action (pg. 8), "seven bits of the effective address are used to generate a seven bit address to access look up table." Accordingly, Doing does not teach that a

number of effective address bits are used to generate a lesser number of address bits that may be used for a reduced linear address.

Since features of the independent claims 1, 11, 17, and 25 are neither taught nor suggested by Going, reconsideration and withdrawal of the rejection of these claims as well as dependent claims 1-5, 11, 17-19 and 25-27 under 35 U.S.C. § 102(b) is respectfully requested.

CONCLUSION

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (202) 220-4255 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,
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